CLAIMS

What is claimed is:

1. A data-flow and context-flow data processing system comprising a plurality of data driven cores capable of switching between a plurality of contexts, wherein the plurality of data driven cores comprises a plurality of distributed multi-context storage units each capable of storing a plurality of context parameters corresponding to the plurality of contexts, each multi-context storage unit comprising:

a) a context register bank comprising

a plurality of context parameter registers for storing the plurality of context parameters, each context parameter register storing a parameter for one of the contexts, the plurality of context parameter registers having a corresponding plurality of inputs connected to an input connection, and a corresponding plurality of outputs; and

a multiplexer having a plurality of multiplexer inputs each connected to a corresponding one of the plurality of context parameter register outputs, for selecting a current context parameter set for transmission to a multiplexer output;

b) a context identification register connected to the context register bank, for storing a current context identification token identifying a current context for the context register bank, wherein

the context identification register is connected to a select line of the multiplexer, for controlling the multiplexer to select the

current context parameter set for transmission; and

the context identification register is connected to a load enable line of each of the context parameter registers, for enabling an updating of a current context parameter set in a corresponding context parameter register; and

c) logic connected to the multiplexer output for receiving the current context parameter set and processing a set of data tokens according to the current context parameter set, connected to the input connection of the context parameter registers for providing updated context parameter sets to the context parameter registers, and connected to the context identification register for propagating the current context identification token through the multi-context storage unit.

2. The system of claim 1, further comprising logic for controlling a flow of the set of data tokens through the cores such that each data token is transferred from a first core to a second core upon a synchronous assertion of a request signal from the second core to the first core, and of a ready signal from the first core to the second core.

3. The system of claim 1, wherein an interface of a core includes a content specification flag for indicating whether a token containing the flag is a data token or a context identification token.

4. The system of claim 1, wherein an interface of a core includes a dedicated context identification field for

transferring a current context identification token with each data token passing through the interface.

5. A data-flow and context-flow data processing system, comprising a plurality of data-driven cores including:

a) logic for controlling a flow of data tokens and context identification tokens through the cores;

b) a plurality of distributed multi-context storage units, each multi-context storage unit including:

a context identification register for storing a context identification token identifying a current context of said each multi-context storage unit; and

a multi-context register bank for storing a plurality of context parameters corresponding to a plurality of contexts,

wherein the context identification register is connected to the multi-context register bank for setting the multi-context register bank to the current context; and

c) logic for processing the data tokens according to a context parameter corresponding to the current context.

6. A data-flow and context-flow data processing system, comprising a plurality of data-driven cores, each of the cores including:

a) a context identification storage unit for storing a current context identification token; and

b) logic for controlling a flow of the current context identification token through the cores such that the current context identification token is transferred from a first core to a second core upon a synchronous assertion of a request signal from the

second core to the first core, and of a ready signal from the first core to the second core.

7. A data- and context-flow processing method comprising the steps of:

a) propagating a current context identification token through a plurality of data flow cores integrated on a chip, the current context identification token identifying a current context;

b) retrieving a set of context parameters corresponding to the current context from each of a plurality of multi-context storage units distributed through the cores, as the current context identification token propagates through the multi-context storage units; and

c) processing a set of data tokens in the current context, according to the set of context parameters.

8. A data- and context-flow data processing system comprising a first data- and context-flow core and a second data- and context-flow core integrated on a chip, the first core comprising:

a) an input interface for receiving a data token and a context identification token from the second core, the context identification token identifying one of a plurality of contexts as a current context, wherein each token transfer between the second core and the first core occurs upon a synchronous assertion of a request signal from the first core to the second core and a ready signal from the second core to the first core;

b) a context identification register connected to the input interface, for storing the context identification token;

c) a multi-context storage unit connected to the context identification register, for storing a plurality of context parameters corresponding to the plurality of contexts;

d) control and processing logic connected to the context identification register and the context register bank, for

9. A data- and context-flow data processing system comprising a plurality of cores, each of the cores comprising:

a) an input control bus for transferring input control signals;

b) an input token bus for receiving input tokens in response to assertions of the input control signals, the input tokens including
an input data token to be processed by the core, and
an input context identification token for specifying a current context;

c) an output control bus for transferring output control signals; and

d) an output token bus for sending output tokens in response to assertions of the output control signals, the output tokens including
an output data token derived from the input data token, and
an output context identification token equal to the input context identification token, for specifying the current context.

10. A multithreaded data processing system comprising a first data-driven core, a second data-driven core, and a third data-driven core integrated on a chip, the first core comprising:

a) a first input interface connected to the second core, comprising

a first input request connection for asserting a first input request signal to the second core,

a first input ready connection for receiving a first input ready signal asserted by the second core, and

a first input data connection for receiving from the second core an input context token for establishing a context state for the first core;

b) processing logic connected to the first input interface, for processing a data token according to the context state;

c) a first output interface connected to the third core, comprising

a first output request connection for receiving a first output request signal asserted by the third core,

a first output ready connection for asserting a first output ready signal to the third core, and

a first output data connection connected to the processing logic, for transmitting to the third core a first output context token derived from the first input token, for establishing the context state for the third core;

d) first input control logic connected to the first input interface, for controlling the first core to receive the first input context token if the first input request signal and the first input ready signal are asserted with a predetermined synchronous relationship; and

e) first output control logic connected to the first output interface, for controlling the first core to transmit the first output context token to the third core if the first output request signal and the first output ready signal are asserted with a predetermined synchronous relationship.

11. The system of claim 10 wherein:

a) the first input control logic comprises logic for controlling the first core to receive the first input context token if the first input request signal and the first input ready signal are asserted synchronously; and

b) the first output control logic comprises logic for controlling the first core to transmit the first output context token to the third core if the first output request signal and the first output ready signal are asserted synchronously.

12. The system of claim 11 wherein:

a) the first input control logic comprises logic for controlling the first core to receive the first input context token synchronously with the first input request signal and the input ready signal; and

b) the first output control logic comprises logic for controlling the first core to transmit the first output context token synchronously with the first output request signal and the output ready signal.

13. The system of claim 10 wherein:

a) the first core further comprises a second output interface connected to a fourth core integrated on the chip, the second output interface comprising
a second output request connection for receiving a second output request signal asserted by the fourth core,
a second output ready connection for asserting a second output ready signal to the fourth core, and
a second output data connection connected to the data processing logic, for transmitting the output context token to the fourth core; and

b) the first core further comprises second output control logic connected to the second output interface, for controlling the first core to transmit the output context token to the fourth core if the second output request signal and the second output ready signal are asserted synchronously.

14. The system of claim 10, wherein the first core further comprises a multi-context storage unit connected to the processing logic, for storing a plurality of context parameters corresponding to a plurality of contexts.

15. The system of claim 14 wherein the multi-context storage unit comprises:

a) a plurality of registers connected in parallel, for storing a plurality of context parameter values for a corresponding plurality of contexts; and

b) a multiplexer connected to the outputs of the plurality of registers, for selecting for transmission a value of the context parameter

corresponding to a current context state for the multi-context storage unit.

16. A multithreaded data processing system comprising a first data-driven core and a second data-driven core, the first core comprising an input interface connected to the second core, the input interface including:
    a) an input request connection for asserting an input request signal to the second core;
    b) an input ready connection for receiving an input ready signal asserted by the second core; and
    c) an input data connection for receiving from the second core, upon a synchronous assertion of the input request signal and the input ready signal, a first input context identification token identifying a current context state.

17. A multithreaded data processing system comprising a first data-driven core, a second data-driven core, and a third data-driven core integrated on a chip, the first core comprising:
    a) an input interface connected to the second core, comprising
        a control bus for transmitting a set of first control signals between the first core and the second core, and
        an input data bus for receiving from the second core, upon the assertion of the set of first control signals according to a predetermined protocol
            an input data token, and
            an input context identification token for establishing a current context state in the first core;

b) processing logic connected to the first input interface, for generating an output data token from the input data token according to the context state; and

c) an output interface connected to the third core, comprising

an output control bus for transmitting a set of second control signals between the first core and the third core, and

an output data bus connected to the processing logic, for transmitting to the third core, upon the assertion of the set of first control signals according to the predetermined protocol the first output token, and

a first output context token derived from the first input token, for establishing the current context state in the third core.

18. A data- and context-flow data processing method comprising the steps of:

a) establishing a first data- and context-driven core and a second data- and context-driven core, the second core being connected to the first core for receiving data tokens and context tokens from the first core; and

b) operating the first core in a first context, and concurrently, operating the second core in a second context different from the first context.

19. A data- and context-flow processing method comprising the steps of:

a) establishing a data- and context-driven core comprising a plurality of interconnected pipestages, the pipestages including

logic for controlling a flow of data tokens and context identification tokens therethrough, and

a plurality of distributed multi-context storage units each storing a plurality of context parameters and each responsive to the context identification tokens; and

b) operating a first set of pipestages in a first context specified by a first context identification token present within the first set of pipestages, and concurrently, operating a second set of pipestages in a second context specified by a second context identification token present within the second set of pipestages.